

AUG 05 2005

Form PTO-1449		U.S. Department of Commerce Patent and Trademark Office						Atty. Docket No. P24677	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)								Applicant Ryutaro YAMANAKA et al	COPY
								Filing Date December 31, 2003	Group Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER							DATE	NAME		CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DR	6	1	9	5	7	8	2	02/27/01	RAHMATULLAH et al	714	795		
DR	6	2	5	7	7	5	6	07/10/01	ZARUBINSKY et al	↑			
DR	6	4	7	7	6	6	1	11/05/03	YAMANAKA				
DR	5	6	3	3	8	9	7	05/27/97	FETTWEIS et al				
DR	5	9	2	3	7	1	3	07/1999	HATAKEYAMA				
DR	5	3	2	7	4	4	0	07/1999	FREDRICKSON et al				
DR	5	9	1	2	9	0	8	06/1999	CESARI et al				
DR	5	9	8	7	4	9	0	11/1993	ALIDINA et al				
DR	5	2	2	0	5	7	0	06/1993	LOU et al				
DR	5	4	1	4	7	3	8	05/1995	BIENZ				
DR	5	7	1	0	7	8	4	01/1998	KINDRED et al	↓	↓		
DR	5	0	2	7	3	7	4	01/1991	ROSSMAN	714	795		

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER							DATE	COUNTRY		CLASS	SUBCLASS	TRANSLATION YES NO	
NOT provided	0	9	-	1	4	8	9	4	3	06/06/97	JAPAN			X
NOT provided	6	3	-	2	1	5	2	2	7	09/07/88	JAPAN			X
NOT provided	6	-	1	6	4	4	2	3		06/10/94	JAPAN			
NOT provided		8	-	8	4	0	8	2		09/14/94	JAPAN			
NOT provided		9	-	1	4	8	9	4	3	11/17/95	JAPAN			
NOT provided	1	0	-	1	0	7	6	5	1	04/24/98	JAPAN			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

1	English Language Abstract JP 09-148943.
2	English Language Abstract JP 63-215227.
3	UEDA et al., "A 16-bit Digital Signal Processor with Specially Arranged Multiply-Accumulator for Low Power Consumption", IEICE Trans. Electron., Vol. E78-C, No. 12, December 1995.

EXAMINER

DATE CONSIDERED

10/6/03

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
lll	4	6	0	6	0	2	7	09/1986	OTANI	714	795	
lll	5	7	4	2	6	2	1	08/1998	AMON et al	↑	7	
lll	6	2	6	3	4	7	4	07/17/01	WATANABE	↑	7	
lll	5	8	8	1	1	0	6	03/09/99	CARTIER	↑	7	
lll	6	3	3	0	6	8	4	12/2001	YAMANAKA et al	↑	7	
lll	5	8	0	9	0	7	1	09/1998	KOBAYASHI et al	↑	7	
lll	5	5	0	9	0	2	1	04/1996	TODOROKI	↑	7	
lll	5	5	0	2	7	3	5	03/1996	COOPER	↑	7	
lll	5	3	7	5	1	2	9	12/1994	COOPER	↑	7	
lll	5	3	7	9	3	0	6	01/1995	NOMA et al	↑	7	
lll	4	6	1	4	9	3	3	09/1986	YAMASHITA et al	↑	795	
lll	6	1	2	5	1	5	3	09/26/00	SUGISAWA et al	714	795	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
lll	1	0	-	2	0	9	8	8	2	08/07/98	JAPAN	
lll	1	1	-	5	5	1	3	0	02/26/99	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

4	H. LOU, "Viterbi Decoder Design for the IS-95 CDMA Forward Link", IEEE 46th Vehicular Technology Conference, No. 2, 1996, pp.1346-1350.
5	English Language Abstract of JP6-164423.
6	English Language Abstract of JP8-84082.
7	English Language Abstract of JP9-148943.
8	English Language Abstract of JP10-107651.
9	English Language Abstract of 10-209882.
10	English Language Abstract of 11-55130.

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